IN THE CLAIMS

Please amend the claims as follows.

1. (Currently Amended) A current reference comprising:

a current mirror circuit to force a first current to be substantially equal to a second current;

a control transistor coupled to the current mirror circuit to receive the first current, the control transistor having first and second biasing terminals across which a biasing voltage can be applied;

a variable resistor including a plurality of parallel binary weighted transistors coupled between the first and second biasing terminals of the control transistor and coupled to the current mirror to receive the second current; and

a control loop responsive to a generated current equal to one of the first and second currents to influence the biasing voltage.

2. (Currently Amended) A current reference comprising:

a current mirror circuit to force a first current to be substantially equal to a second current;

a control transistor coupled to the current mirror circuit to receive the first current, the control transistor having first and second biasing terminals across which a biasing voltage can be applied;

a variable resistor coupled between the first and second biasing terminals of the control transistor and coupled to the current mirror to receive the second current; and

a control loop responsive to a generated current equal to one of the first and second currents to influence the biasing voltage, ~~The current reference of claim 1~~ wherein the variable resistor comprises a plurality of resistive devices in parallel, each of the plurality of resistive devices having a control input node to enable the resistive device.

3. (Currently Amended) A current reference comprising: